WHAT IS CLAIMED IS:

1. A processor comprising:

a register; and

an execution core coupled to said register, wherein said execution core is configured to execute an instruction to produce a result, said instruction having said register as a destination, and wherein said execution core is configured to selectively zero extend said result for update in said register responsive to an operand size corresponding to said instruction.

2. The processor as recited in claim 1 wherein said result comprises a number of bits specified by said operand size.

3. The processor as recited in claim 2 wherein said operand size comprises one of a first size, a second size greater than said first size, a third size greater than said second size, and a fourth size greater than said third size.

4. The processor as recited in claim 3 wherein said register is capable of storing operands of said fourth size.

5. The processor as recited in claim 3 wherein said execution core is configured to zero extend said result if said operand size is said third size, and wherein said execution core is configured not to zero extend said result if said operand size is said first size or said second size.

6. The processor as recited in claim 5 wherein said execution core is configured to preserve a value in at least a portion of a remainder of said register if said operand size is

said first size or said second size.

7. The processor as recited in claim 3 wherein said first size is eight bits, said second size is 16 bits, said third size is 32 bits, and said fourth size is 64 bits.

8. The processor as recited in claim 1 wherein said execution core is coupled to receive an operating mode of said processor, and wherein said execution core is configured to selectively zero extend said result further responsive to said operating mode.

9. The processor as recited in claim 8 wherein said operating mode includes a default operand size, and wherein said operand size corresponding to said instruction is said default operand size unless overridden by said instruction's encoding.

10. The processor as recited in claim 9 wherein said execution core is configured to zero extend said result if said operand size is said default operand size.

11. The processor as recited in claim 9 wherein said default operand size is overridden by said instruction's encoding if said instruction includes one or more operand size override prefixes.

12. The processor as recited in claim 1 wherein said execution core is configured to preserve a value in at least a portion of a remainder of said register if not zero extending said result.

13. A method comprising:

executing an instruction to produce a result, said instruction having a register as a destination; and

selectively zero extending said result for update in said register responsive to an operand size corresponding to said instruction.

14. The method as recited in claim 13 wherein said result comprises a number of bits specified by said operand size.

15. The method as recited in claim 14 wherein said operand size comprises one of a first size, a second size greater than said first size, a third size greater than said second size, and a fourth size greater than said third size, and wherein said selectively zero extending comprises:

zero extending said result if said operand size is said third size; and

not zero extending said result if said operand size is said first size or said second size.

16. The method as recited in claim 15 further comprising preserving a value in at least a portion of a remainder of said register if said operand size is said first size or said second size.

17. The method as recited in claim 13 wherein said selectively zero extending is further responsive to an operating mode of a processor performing said executing.

18. The method as recited in claim 17 wherein said operating mode includes a default operand size, wherein said selectively zero extending further comprises zero extending said result if said operand size is said default operand size.

19. The method as recited in claim 13 further comprising preserving a value in at least a portion of a remainder of said register if not zero extending said result.